Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A process for manufacturing an electronic semiconductor device, comprising:

forming a body of semiconductor material having an array portion and a circuitry portion;

forming a gate electrode of a semiconductor material on top of said circuitry portion;

forming a first silicide protection mask on top of said array portion simultaneously with said step of forming said gate electrode;

silicidating said gate electrode; and

removing said first silicide protection mask.

2. (Original) A process according to claim 1, wherein said steps of forming a first silicide protection mask and a gate electrode comprise:

depositing a polysilicon layer;

selectively removing portions of said polysilicon layer; and

forming both said gate electrode and said first silicide protection mask from said polysilicon layer.

3. (Original) A process according to claim 2, wherein, before depositing a polysilicon layer, an oxide layer is formed onto said body and, after removing said polysilicon layer, uncovered portions of said oxide layer are removed.

4. (Original) A process according to claim 1, further comprising the step of forming a second silicide protection mask covering said first silicide protection mask before said step of silicidating said gate electrode.

5. (Original) A process according to claim 4, further comprising forming spacers laterally to said gate electrode, said step of forming spacers being performed simultaneously to said step of forming a second silicide protection mask.

6. (Original) A process according to claim 5, wherein said step of forming spacers and a second silicide protection mask comprises:

forming a dielectric layer on top of said body,

protecting said array portion using an array mask,

anisotropically etching exposed portions of said dielectric layer; and

forming both said spacers and said second silicide protection mask from said dielectric layer.

7. (Original) A process according to claim 6, wherein said dielectric layer is of a material selected from oxide, nitride and a superposition of oxide and nitride.

8. (Original) A process according to claim 4, comprising, after said step of silicidating said gate electrode, removing said second silicide protection mask.

9. (Currently Amended) A process according to claim 8, wherein said second silicide protection mask has an edge portion extending on a lateral side of said first silicide protection mask on top of ~~said~~ an insulating region forming in said body around the array portion, and wherein said steps of removing said first silicide protection mask and removing said second silicide protection mask comprise:

forming a circuitry mask covering said circuitry portion and part of said insulating region so that an edge of said circuitry mask extends on a central portion of said insulating region and on a part of said edge portion of said second silicide protection mask; and

etching uncovered portions of said first and second silicide protection masks.

10. (Original) A process according to claim 1, further comprising, after said step of removing said first silicide protection mask:

forming a nitride borderless layer;

forming an upper insulating layer on said body;

forming openings in said upper insulating layer and said nitride borderless layer; and

implanting conduction regions in said array portion.

11. (Original) A process according to claim 10, further comprising the step of forming PCM elements of a chalcogenic material in said upper insulating layer.

12. (Original) A process according to claim 1, further comprising the step of forming at least one insulating region in said body around said array portion.

13. (New) A process for manufacturing a semiconductor device comprising:

forming a body of semiconductor material having an array portion and a circuitry portion;

forming an insulating region in said body around the array portion, said insulating region having a central portion and a border portion abutting said array portion;

forming a gate electrode of a semiconductor material on top of said circuitry portion;

forming a first silicide protection mask simultaneously with said step of forming said gate electrode, said first silicide protection mask covering the entire said array portion and

having a top and a lateral side, said lateral side reaching on top of the border portion of said insulating region;

forming a spacer on a side of said gate electrode;

forming a second silicide protection mask covering the top and the lateral side of said fist silicide protection mask, said second silicide protection mask reaching on top of the central portion of said insulating region; and

silicidating said gate electrode.

14. (New) The process of claim 13 wherein the first silicide protection mask is polysilicon.

15. (New) The process of claim 13 wherein the second silicide protection mask is a sacrificial oxide layer.

16. (New) The process of claim 13 wherein the second silicide protection mask is a sacrificial nitride layer.

17. (New) The process of claim 13, further comprising, after said step of silicidating said gate electrode:

removing said first and second silicide protection masks;

forming a nitride borderless layer;

forming an upper insulating layer on said body;

forming openings in said upper insulating layer and said nitride borderless layer; and

implanting conduction regions in said array portion.

18. (New) A process according to claim 16, further comprising the step of forming PCM elements of a chalcogenic material in said upper insulating layer.